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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/549,996	09/19/2005	Joji Fujiwara	MAT-8744US	1009
52473	7590	10/07/2008	EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/549,996	FUJIWARA ET AL.	
	Examiner	Art Unit	
	LATANYA CRAWFORD	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on 29 May 2008.
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1,3,5,6,8 and 10-24 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1,3,5,6,8 and 10-24 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 19 September 2005 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____ .
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)	5) <input type="checkbox"/> Notice of Informal Patent Application
Paper No(s)/Mail Date _____.	6) <input type="checkbox"/> Other: _____ .

DETAILED ACTION

1. This office action is in response to the correspondence filed on 05/29/2008.

Currently, claims 1, 3, 5, 6, 8, 10-24 are pending.

Specification

2. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter. See 37 CFR 1.75(d)(1) and MPEP § 608.01(o). Correction of the following is required: The specification does not specifically have the content of "a first sealing member", "a second sealing member" as mentioned in claims 1-3, 17, & 18. The specification does not specifically have the content of "a first conductive film" and "a second conductive film" as mentioned in claims 1,14, 16, 17, 20-24. The specification does not specifically have the content of claims 23 & 24, "wherein the first conductive film and the second conductive film have ends which face the partition and which are separated by the partition". Furthermore, the specification does not specifically have the content of "the partition is higher than an electric component mounted on the substrate" as mentioned in claims 15 & 17.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1 & 8-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US Pub no. 2004/0252475 A1).

Regarding claim 1, Tsuneoka et al. discloses a substrate(10) a partition (70- sealing body and metal film 20 provided on the vertical sides of 70) formed on the substrate (10), the partition having a predetermined height to divide the substrate into a plurality of circuit blocks (fig. 5);a first sealing member (40)covering a first circuit block of the plurality of circuit blocks and a second sealing member (40)covering a second circuit block of the plurality of circuit blocks fig. 5; a first conductive film (20) covering at least a surface of the first sealing member; and covering at least a surface of the second sealing member; wherein the plurality of circuit blocks are electrically shielded individually and the partition is made of a composition of a resin and an electrically conductive material (70- sealing body and metal film 20 provided on the vertical sides of 70) fig. 5 [0025]. Examiner notes that, the limitation of Claim 1 wherein a second conductive film covering at least a surface of the second sealing member would be *prima facie* obvious for one of ordinary skill in the art at the time of the invention, since it has been held that constructing a formerly integral structure, such as the first conductive film of Tsuneoka et al., into a structure of various elements involves only routine skill in the art (*Nerwin v. Erlichman*, 168 USPQ 177, 179). A *prima facie* case of obviousness thereby exists for this limitation (See MPEP § 2142 and § 2144.04).

Regarding claim 8, Tsuneoka et al. teaches the partition 70 has a conductive wall 20 in a direction vertical to the substrate 10 (view fig. 5).

Regarding claim 9, Tsuneoka et al. teaches the partition is formed by stacking at least one metal film 20 and ,resin 70; and the metal film is formed to be parallel with the longitudinal direction of the partition 70 and to be vertical to the substrate 10 (fig 5).

Regarding claim 10, Tsuneoka et al. teaches the partition 70 has resin at least one side surface thereof (view fig. 5).

Regarding claim 11, Tsuneoka et al. teaches the partition 70 is positioned inside the substrate 10, and has a planar shape of one of a circle or polygon (fig. 6).

Regarding claim 12, Tsuneoka et al. teaches the partition 70 is positioned out of contact with an outer edge of the substrate 10 (fig. 5).

Regarding claim 13, Tsuneoka et al. teaches the partition 70 has a planar shape of a letter T (fig. 4).

Regarding claim 14, Tsuneoka et al. teaches the first conductive film and the second conductive film 20 include metal [0024] fig. 5.

Regarding Claim 15,Tsuneoka et al. discloses the partition 70 is higher than an electric component mounted 30 on the substrate 10 (view fig. 5).

Regarding claim 16, Tsuneoka et al. teaches the substrate 10 has a ground pattern 50 on a surface thereof, and the ground pattern 50 is connected with the first conductive film 20 fig. 5 [0018]. Examiner notes that, the limitation of Claim 16, a second conductive film connected to the ground pattern would be *prima facie* obvious for one of ordinary skill in the art at the time of the invention, since it has been held that constructing a formerly integral structure, such as the first conductive film of Tsuneoka et al., into a structure of various elements involves only routine skill in the art (*Nerwin v.*

Erlichman, 168 USPQ 177, 179). A prima facie case of obviousness thereby exists for this limitation (See MPEP § 2142 and § 2144.04).

5. Claims 2, 5, 6, & 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US 2004/0252475 A1) in view of Mathews (US Patent 7,049,682 B1).

Regarding claim 2, Tsuneoka et al. discloses all the claim limitations of claim 1 and further teaches the substrate 10; the first sealing member, the second sealing member 40 (first and second portion of element 40, in fig. 5) and the partition 70 contain the same resin [0028] but fails to teach that the substrate is made of resin.

However, Mathews et al. teaches the substrate is made of resin (column 3, lines 37-40). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with the substrate made of resin taught by Mathews et al. since doing so would provide mounting means for electronic components.

Regarding claim 5, Tsuneoka et al. teaches the conductive material of the partition 70 is a conductive resin ([0028], lines 1-9).

Regarding Claim 6, Tsuneoka et al. discloses all of the claimed limitations from and further teaches the partition 70 is resin having a metal film 20 formed on an outer surface thereof (fig. 5) except for having a square cross section in a longitudinal direction. The partition having a square cross section in a longitudinal direction is a matter of design choice where a person of ordinary skill in the art would have found obvious absent persuasive evidence that the particular configuration of the partition was significant. In re Dailey 357 F.2d 669.149 USPQ 47 (CCPA 1966).

Regarding claim 23, Mathews et al. teaches the first conductive film (162) and the second conductive film (162) have ends which face the partition (620/ and inner vertical portions of 162) and which are separated by the partition fig. 6(Examiner notes that the outer vertical portions of 162 have an inner edge represents the ends of the first and second conductive film such that they are separated by the partition as shown in fig. 6).

6. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US 2004/0252475 A1) in view of Nakatani (US Patent 6,734,542 B2).

Regarding claim 3, Tsuneoka et al. discloses all the claim limitations of claim 1 but fails to teach wherein the substrate is ceramic; the composition is made of ceramic powder-containing resin and conductive material; and the first sealing member, the second sealing member and the partition contain the same resin.

However, Nakatani et al. teaches the substrate is ceramic 809; the composition is made of ceramic powder-containing resin and conductive material (column 16, lines 33-40); and the first sealing member, the second sealing member 805 and the partition 804 contain the same resin (fig. 8; column 16, lines 18-20; column 15, lines 48-51). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with the substrate is ceramic; the composition is made of ceramic powder-containing resin and conductive material; and the first sealing member, the second sealing member and the partition contain the same resin taught by Nakatani et al. since it would be possible to control the thermal conductivity, the coefficient of thermal expansion, and the dielectric constant.

7. Claims 21 & 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US 2004/0252475 A1) in view of Nakatani (US Patent 6,734,542 B2).

Regarding claim 21, Tsuneoka et al. discloses all the claim limitations of claim 1 but fails to teach wherein the first and second conductive films are separated by the partition

However, Nakatani et al. teaches the first and second conductive films (top and bottom wiring pattern 801) are separated by the partition (804) (fig. 8; column 16, lines 18-20 & column 14, lines 8-11). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with the first and second conductive films are separated by the partition taught by Nakatani et al. since doing so would have been a matter of design choice.

Regarding claim 22, Nakatani et al. discloses wherein the partition 804 electrically connects the first conductive film with the second conductive (top and bottom wiring pattern 801) (fig. 8; column 16, lines 18-20 & column 14, lines 8-11).

8. Claims 17, 18, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US Pub no. 2004/0252475 A1).

Regarding claim 17, Tsuneoka et al. discloses a method for manufacturing a module component having a plurality of circuit blocks shielded individually, the method comprising: a step of mounting a partition made of resin and an electrically conductive material70- sealing body and metal film 20 provided on the vertical sides of 70) higher than mounting components (30), the partition 70- sealing body and metal film 20

provided on the vertical sides of 70) dividing the mounting components and a substrate into a plurality of circuit blocks on the substrate (10)fig. 5, a step of forming a first sealing member (40) covering a first circuit block of the plurality of circuit blocks individually in such a manner as to be higher than the mounting components (30); a step of forming a second sealing member (40) covering a second circuit block of the plurality of circuit blocks individually in such a manner as to be higher than the mounting components (30) fig. 5; step of forming a first conductive film on a surface of the first sealing member (40) and on a surface of the second sealing member (40) fig. 5.

Examiner notes that, the limitation of Claim 16, a second conductive film on a surface of the second sealing member would be *prima facie* obvious for one of ordinary skill in the art at the time of the invention, since it has been held that constructing a formerly integral structure, such as the first conductive film of Tsuneoka et al., into a structure of various elements involves only routine skill in the art (*Nerwin v. Erlichman*, 168 USPQ 177, 179). A *prima facie* case of obviousness thereby exists for this limitation (See MPEP § 2142 and § 2144.04).

Regarding claim 18, Tsuneoka et al. discloses the partition 70 contains a conductive material [0028] formed in a direction vertical to the substrate 10 (fig. 5); and the step of forming a first sealing member 40 fig. 5

Regarding claim 20, Tsuneoka et al. discloses the step of forming a first conductive film 20 fig. 5 or the step of forming a second conductive film includes a step of connecting the respective conductive film with a ground pattern 50 fig. 5[0026]

9. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US Pub no. 2004/0252475 A1) in view of Percival (US Patent 4,691,434).

Regarding claim 19, Tsuneoka et al. discloses all of the claimed limitations from claim 17 above but fails to teach a step of removing the conductive material by one of dicing and laser.

However, Percival et al. teaches a step of removing the conductive material by one of dicing and laser (Abstract, lines 8-14). It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the module component of Tsuneoka et al. with removing the conductive material by laser taught by Percival et al. since doing so provides connections to underlying electronic components.

10. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tsuneoka (US 2004/0252475 A1) in view of Mathews (US Patent 7,049,682 B1).

Regarding claim 24, Tsuneoka et al. discloses all the claim limitations of claim 17 but fails to teach the first conductive film and the second conductive film are formed with ends which face the partition and which are separated by the partition.

However, Mathews et al. teaches the first conductive film (162) and the second conductive film (162) have ends which face the partition (620/ and inner vertical portions of 162) and which are separated by the partition fig. 6(Examiner notes that the outer vertical portions of 162 have an inner edge represents the ends of the first and second conductive film such that they are separated by the partition as shown in fig. 6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the module component of Tsuneoka et al. with the first conductive film and the

second conductive film are formed with ends which face the partition and which are separated by the partition taught by Mathews et al. since doing so would provide shielding.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LATANYA CRAWFORD whose telephone number is (571)270-3208. The examiner can normally be reached on Monday-Friday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571)-272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Supervisory Patent Examiner, Art

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